



AMBA[®] CHI Issue G Errata

Architecture & Technology Group

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AMBA® CHI Issue G Errata

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Chapter 1

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Chapter 2

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Preface

This document lists errata on the AMBA CHI Issue G specification [\[1\]](#).

Each errata description is organized as a brief reason for the change, along with the precise change.

Errata classification

Each listed errata has a classification ID, of the form XYYY, where:

X is the errata classification type as follows, C, R, E or D:

C	Clarification	Informative change only
R	Relaxation	Backward-compatible normative change, modifying existing functionality
E	Enhancement	Backward-compatible normative change, adding new functionality
D	Defect	Non-backward compatible normative change

YYY is an Arm internal tracking number.

Additional reading

This section lists publications by Arm and by third parties.

See Arm Developer (<http://developer.arm.com>) for access to Arm documentation.

[1] *AMBA 5 CHI Architecture Specification*. (ARM IHI 0050 G) Arm Ltd.

Chapter 1

New/Updated Errata

1.1 R858: BROADCASTMTE effect on MTE fields relating to previously cached locations

Affects:

CHI-E.a, CHI-E.b, CHI-E.c, CHI-F, CHI-F.b, CHI-G

Description:

When the MTE feature was introduced into CHI-E, a **BROADCASTMTE** pin was also included to control the MTE-related fields in messages. The intent of this signal is to ensure that Tag-related operations are not issued to downstream components that do not support MTE. It is expected that this pin will control the main functional logic of the component, but not necessarily the caches that exist towards the external interface of that component.

The MTE feature allows a request with `TagOp=Invalid` to see the corresponding data returned with `TagOp=Transfer`, indicating that Clean tags are included.

If a component that supports MTE has the **BROADCASTMTE** pin deasserted, it is possible for that component to cache Clean tags returned to a read request issued with `TagOp=Invalid`. When the data for that location is later sent downstream as a result of an eviction, or returned as a result of a snoop, it is possible for the data to be transferred along with the Clean tags. This should not cause a problem for the interconnect, as to receive the Clean tags in the first instance, it must already support MTE. It is always OK for a Requester to ignore or drop Clean tags that are returned to it.

Implementations are not expected to zero the MTE related fields when data allocated into the local cache is later transferred elsewhere. The previous wording for the **BROADCASTMTE** pin is considered too strict, and will be updated.

The precise change(s):

The text that currently describes **BROADCASTMTE**, in section B16.2.6 of CHI-G on page 537 will be updated.

From:

The **BROADCASTMTE** signal is used to control the issuing of requests with MTE beyond the interface:

- When asserted, requests with MTE can be sent beyond the interface.
- When deasserted, requests with MTE must not be sent beyond the interface.

The **BROADCASTMTE** signal is typically deasserted when the interface does not support MTE functionality.

When the **BROADCASTMTE** signal is deasserted, all other MTE-related interface pins must be tied to 0. The interconnect is permitted, but not required, to remove the related MTE transport wires.

The interface fields that can be fixed to a value of 0 are:

- On DAT channels:
 - TagOp, Tag, and TU
- On REQ and RSP channels:
 - TagOp

To:

The **BROADCASTMTE** signal is used to control the value of MTE related fields in messages beyond the interface except for those relating to evictions or snoop responses for cached data.

- When asserted, all messages with MTE can be sent beyond the interface.
- When deasserted:
 - In the following outbound REQ and DAT messages from a Requester Node, TagOp is permitted to be *Invalid* or *Transfer*:
 - Cache evictions, and any associated data transfers
 - SnpRespData, SnpRespDataFwdded, and CompData in response to a snoop
 - In outbound DAT messages:
 - When TagOp is *Transfer*, Tag is permitted to be non-zero.
 - When TagOp is *Invalid*, Tag must be zero.
 - The TU field must be zero.
 - TagOp must be *Invalid* in:
 - All other outbound messages from a Requester Node.
 - All outbound messages from a Home Node.

Note Cache evictions can be:

- Snoopable cache evictions for locations cached following Allocating Reads:
 - CopyBack Write
 - Combined CopyBack Write and CMO
- Non-snoopable cache evictions for locations cached following ReadNoSnp transactions:
 - WriteNoSnp
 - Combined WriteNoSnp and CMO

When **BROADCASTMTE** is deasserted it remains possible for cache evictions and snoop responses to be issued with MTE-related interface fields not set to 0. This can occur when a read issued with TagOp=*Invalid* sees the corresponding data returned with TagOp=*Transfer*, indicating Clean tags are included. If those Clean tags are cached, an implementation is expected, but not required, to zero out them out again when issuing a later CopyBack/WriteNoSnp of the line, or responding to a snoop that targets the cached line.

For the Requester to receive MTE tags, the interconnect must already be supporting MTE, so the later issuing of these tags will not cause any system issues.

The **BROADCASTMTE** signal is typically deasserted when the connecting interface does not support MTE functionality.

1.2 R907: When MEC_Support is False, MECID_Width can be non-zero

Affects:

CHI-G

Description:

When the *Memory Encryption Contexts* (MEC) feature was introduced, two additional properties were defined:

- MEC_Support
- MECID_Width

Rules were included that stated if MECID_Width was non-zero, then the MEC_Support property must be true. This is too restrictive as implementations might want to build in reset time configuration options that allow for the disabling of a feature property, whilst still keeping the associated fields present.

The rules will be relaxed so that the MECID_Width property being non-zero does not mandate the functionality associated MEC_Support.

For the MEC_Support feature property to be true, MECID field presence will still remain a requirement.

The precise change(s):

The following text on page 533 of the CHI-G specification will be updated from:

The MECID_Width parameter has the following conditions:

- If MEC_Support is False, MECID_Width must be 0
- If MEC_Support is True, MECID_Width must not be 0.

To:

The MECID_Width parameter has the following conditions:

- If MEC_Support is True, MECID_Width must not be 0.
- If MEC_Support is False, MECID_Width can take any permitted value.

Additionally, the “False or Not specified” row in Table B16.25 (MEC_Support property options) on page 532 will be updated to remove the following statement:

No MECID fields are present on the interface.

1.3 C925: Resp can be non-Invalid in response to StashOnce*

Affects:

CHI-B, CHI-C, CHI-D, CHI-E.a, CHI-E.b, CHI-E.c, CHI-F, CHI-F.b, CHI-G

Description:

Cache stashing is a feature that was first introduced into CHI in issue B. The Completion response, Comp, to an independent Stash request is permitted to have a Resp value other than 0b000 (Invalid). The Resp value in the Comp response can be used to indicate the state of the cache line at the next level. This information might be useful for the tuning of HW prefetchers for example. If the prefetcher establishes that many of the previous stashes to the SLC were already present there prior to the StashOnce transactions being issued, then it could be considered that future StashOnce transactions to other locations might not be needed.

There have been contradictory statements in the CHI specifications to this point, some which permitted a non-zero Resp value in Comp for independent Stash transactions, and others which stated it must be 0b000 (Invalid).

Updates will be made to permit non-zero Resp values in Comp responses for independent Stash transactions.

The precise change(s):

The following text in section B4.5.1.2 (Dataless transaction completion) of CHI-G, on page 225, will be updated from:

Cache state The final state the cache line is permitted to be in at the Requester, except for CMO transactions. For CMO transactions, the cache state field value in the completion, specifically in Comp, CompCMO and CompPersist transactions, is ignored and the cache state remains unchanged.

To:

Cache state The final state the cache line is permitted to be in at the Requester, except for CMO transactions and StashOnce* transactions.

- For CMO transactions, the cache state field value in the completion, specifically in Comp, CompCMO and CompPersist responses, is ignored and the cache state remains unchanged.
- For StashOnce* transactions, the cache state field value in the Comp and CompStashDone responses is permitted, but not required, to be used to indicate the presence of the cache line at the next level. See section B7.3 for more information.

Table B4.27 (Permitted Dataless transaction completion and Resp field encodings) will be updated to permit Comp_SD from the next level cache in response to a StashOnce transaction.

Table 1.1: Permitted Dataless transaction completion and Resp field encodings

Response	Resp[2:0]	Final cache line state	Notes
Comp_I	0b000	I	
Comp_UC	0b010	UD, UC, UCE, SC, or I	
Comp_SC	0b001	SC or I	
Comp_SD	0b011	N/A	Only used in Comp or CompStashDone for StashOnce transactions.
Comp_UD_PD	0b110	UD or SD	Responsibility for a Dirty cache line is being passed.

Table B13.35 (Valid Resp value encodings for different message types) will have the following text changed from:

Comp responses (Not including WriteNoSnpDef transactions)

To:

Comp responses (Not including WriteNoSnpDef or StashOnce* transactions)

A new major row will then be added to cover the permitted Resp values for StashOnce Comp responses:

Table 1.2: Valid Resp value encodings for different message types

Response type	Resp[2:0]	State	Notes
Comp responses for StashOnce* only	0b000	I	Cache state in the response is imprecise and must be ignored
	0b001	SC	Cache state in the next level cache
	0b010	UC, UD	
	0b011	SD	
	0b100	-	Reserved
	0b101	-	
	0b110	-	
	0b111	-	

1.4 D926: Some Table B10.4 encodings for PAS are incorrect

Affects:

CHI-G

Description:

CHI-G introduced the RME *Coherent Device Assignment* (CDA) feature, which potentially requires the SecSID1 field in device requests to the host. The SecSID1 field qualifies the Security state of the StreamID, which is then used in the translation process to determine the *Physical Address Space* (PAS) that can be accessed.

The table outlining the allowed relationship between SecSID1 and the final PAS mapping contains incorrect encodings for NSE and NS for the specified PAS. These errors will be corrected.

The precise change(s):

Table B10.4 (Field value relationships in a device request to the host) on page 394 of CHI-G will be updated from:

SecSID1	Security state	NSE	NS	PAS	Permitted combination
0b0	Non-Secure	0b0	0b1	Non-secure	Yes
		0b1	0b1	Realm	No
0b1	Realm	0b1	0b0	Non-secure	Yes
		0b0	0b0	Realm	Yes
0bX	Any	0b1	0b1	Root	No
		0b0	0b1	Secure	No

To:

SecSID1	Security state	NSE	NS	PAS	Permitted combination
0b0	Non-Secure	0b0	0b0	Secure	No
		0b0	0b1	Non-secure	Yes
		0b1	0b0	Root	No
		0b1	0b1	Realm	No
0b1	Realm	0b0	0b0	Secure	No
		0b0	0b1	Non-secure	Yes
		0b1	0b0	Root	No
		0b1	0b1	Realm	Yes

Chapter 2

Previous Errata

2.1 None

There are no previous errata.